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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.
09/103,873	06/24/98	NAGANO	Y	YAO-3950

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ANDREW L. NEY
RATNER & PRESTIA
SUITE 301 ONE WESTLAKES BERWYN
P O BOX 980
VALLEY FORGE PA 19482-0980

EXAMINER	
DIAZ, J	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 07/05/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/103,873	NAGANO ET AL.	
	Examiner	Art Unit	
	José R. Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with th corr spond nce addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *11-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 1998* is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☒ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☐ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5,7* .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

Drawings

➢ Figures 10A, 10B, 10C, and 10E should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Claim Rejections - 35 USC § 103

➢ The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

➢ This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102((e), f) or (g) prior art under 35 U.S.C. 103(a).

➢ Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Specification in view of Yoshizumi et al. (US Patent No. 5,444,012) and further in view of Matsuura et al. (US Patent No. 5,132,774).

Regarding claim 1, Applicant acknowledges that is well known in the art to form a semiconductor device comprised of: an integrated circuit (4) on a supporting substrate (1); a capacitor (10) having a lower electrode (7), a dielectric film (8), and an upper electrode (9); a first interlayer insulating film (11); a first interconnect (14) electrically connected to the integrated circuit (4) and the capacitor (10) through a first contact hole (12) formed in the first interlayer insulating film (11); a second interlayer insulating film (15); a second interconnect (15) electrically connected to the first interconnect (14) through a second contact hole (12) formed in the second interlayer insulating film (15); and a passivation layer (18) (Figure 10A-10E).

Regarding claim 2, Applicant acknowledges that the dielectric film (8) is formed either a dielectric material having a high dielectric constant or ferroelectric material (Page 2, lines 26-28).

➢ However, Applicant fails to teach providing the second interconnect on the second interlayer insulating film so as to cover at least a part of the capacitor, a passivation layer that is formed from a laminate including a silicon oxide film and a silicon nitride film, and a hydrogen supplying layer.

Regarding claim 3, Yoshizumi et al. teach providing the second interconnect (DL_1, DL_2) on selective portions of an insulating film (35) so as to cover at least a part of the capacitors (C_1, C_2) (Figure 24).

Regarding claim 4, Yoshizumi et al. teach a passivation layer that is formed from a laminate including a silicon oxide film (37a, 37b) and a silicon nitride film (37c) (Figure 28).

Regarding claims 6 and 10, Yoshizumi et al. teach that the wiring material is a three-layer film formed by successive lamination of TiW film (200c) aluminum alloy film (200b) and TiW (200a) (column 20, lines 54-56).

- However, Yoshizumi et al. fail to teach a hydrogen supplying layer.

Regarding claim 5, Matsuura et al. teach forming a hydrogen supplying layer (13,16) (i.e. nitride layer) to relax the stress of TEOS film (14) (column 7, lines 3-6 and 7-10).

Regarding claim 7, Matsuura et al. teach a Si-OH bond absorption coefficient of the insulating film at a wavelength corresponding to 3450 cm^{-1} is 800 cm^{-1} or less (Figure 3B).

Regarding claim 9, Matsuura et al. teach that it is known in the art to provide an ozone TEOS film having a thickness of about 5 μm (column 1, lines 30-35).

Regarding claim 8, the ozone TEOS film disclosed by Matsuura et al. has the same properties that Applicant intents to claim, hence it is inherent that the second interlayer insulating film of the semiconductor device disclosed by Matsuura et al. has a tensile stress of 1 x 10^7 dyn/cm^2 to 3 x 10^9 dyn/cm^2.

- The claim(s) contain method of making characteristics (i.e. Ozone TEOS) given no patentable weight in determining patentability of the final device structure. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and

particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear.

➢ Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to have modified Applicant to include providing the second interconnect on the second interlayer insulating film so as to cover at least a part of the capacitor, and a passivation layer that is formed from a laminate including a silicon oxide film and a silicon nitride film since such modification would result in a technique which permits ensuring the reliability of the aperture for cutting the fuse and exact judgment a to whether each chip is good or bad while keeping an increasing in the number of manufacturing steps to a minimum, as described in column 5, lines 64-68 of Yoshizumi et al. and to include a hydrogen supplying layer since such modification would result in a semiconductor device having satisfactory insulation by feature of the interlayer insulating film not having cracks as described in column 3, lines 23-25 of Matsuura et al.

Conclusion

➢ The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Konuma et al. (US Patent No. 5,608,251) disclose a thin film

semiconductor integrated circuit. Kanazawa (US Patent No. 5,459,353) discloses a semiconductor device including interlayer dielectric film layers and conductive film layers. Koyama et al. (US Patent No. 5,789,762) disclose a semiconductor active matrix circuit. Mochizuki et al. (US Patent No. 5,990,507) disclose a semiconductor device having ferroelectric capacitor structures. Fujino et al (Conference) disclose a reaction mechanism of TEOS and O_3 atmospheric pressure CVD. H. Wallace Fry et al. disclose application of APCVD TEOS/O_3 thin films in ULSI IC fabrication. Fujino et al. disclose a doped silicon oxide deposition by atmospheric pressure and low temperature chemical vapor deposition using TEOS and ozone. Maeda et al. disclose development history and applications of CVD TEOS/ozone.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 8:00 - 5:00 Monday through Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mahshid Saadat can be reached on (703) 308-4915. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD
June 29, 2000

DAVID HARDY
PRIMARY EXAMINER